DRAM Design Overview

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Contents

• Trends of Standard DRAM
• History of DRAM Circuits
• Cell, Array and Major Circuits
• Embedded DRAM
• ASM Example
• Summary
**Standard DRAM Development**

- **Die Size (mm²)** vs **Year**
  - **Die Size** for various DRAM capacities (16M, 64M, 256M, 1G, 4G)
  - **Rule (µm)** for different generations (i-line, KrF, KrF+, ArF)

**Bit Cost Trend of DRAMs**

- **Density (Mbits)**, **Rule (µm)**, and **Die Size (mm²)** vs **Year**
  - **Density** vs **Year**
  - **Rule** vs **Year**
  - **Bit Cost** vs **Year**

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Access Time Trend

- Power Supply Voltage (V)
- TRAC (RAS Access Time: ns)
- 1/tAA (CAS Access Frequency: MHz)
- f CLK (Popular Synchronous Frequency: MHz)

<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>4M</td>
<td>25</td>
<td>20</td>
<td>15</td>
</tr>
<tr>
<td>16M</td>
<td>12</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>64M</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
</tbody>
</table>

Product Volume [100 million]
**DRAM Operating Frequency v.s. Customizability**

- **Function rich DRAM**: WRAM, CDRAM, VRAM, EDRAM, SDRAM, DDR, RAMBUS, Target
- **High-speed DRAM**: DRAM/Logi
- **Operating Frequency**: 100MHz, 200MHz, 500MHz, 1GHz, 2GHz
- **Customizability**: ASSP/ASIC Standard
- **Bits Density**: 4M, 16M, 256M, 1G, 4G
- **VCC & VII & WL Voltage Trend**:
  - Internally Regulated Supply Voltage (V)
  - Power Supply Voltage (V)
  - Word Boost Level (V)

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**Power Dissipation Trend**

- **Active Power**: tRC=\text{min.} (A)
- **Power Supply Voltage (V)**
- **Stand-by Power** (Low Power mode: mA)

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**Refresh Specification Trend**

- Numbers of Active S/As
- Refresh Cycles
- Refresh Interval (max.:ms)
- Busy Rate (\mu s)
- Distributed Refresh Interval

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**History**

- **1K DRAM**  Intel 1103 introduced late 1971  
  - 3Tr PMOS, 1P1M,  
  - $V_{dd}=0v, V_{ss}=16v, V_{bb}=20v$, $Trac=300ns$

- **4K DRAM**  TI TMS4030 introduced 1973  
  - 1Tr NMOS, 1P1M, TTL I/O  
  - $V_{dd}=12v, V_{dd}=5v, V_{ss}=0v, V_{bb}=-3/-5v$

- **16K DRAM**  Mostek MK4116 introduced 1977  
  - 1Tr NMOS, 2P1M, Address multiplex  
  - $V_{dd}=12v, V_{dd}=5v, V_{ss}=0v, V_{bb}=-5v$, $Trac=250ns$

  **Open / Folded bit line, Double poly cell, Multi-PS**

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**Basic Bitline Structure (1)**

**Open Bitlines**  
- Memory Array  
- BL  
- WL  
- S/As  

**Folded Bitlines**  
- Memory Array  
- BL  
- WL  
- S/As  

**Open BL**  
- Cell Size $6F^2$  
- $WL$ pitch: $3F$  
- $BL$ pitch: $2F$

**Folded BL**  
- Cell Size $8F^2$  
- $WL$ pitch: $4F$  
- $BL$ pitch: $2F$

**Denser Memory**  
- Uneven WL coupling  

**Relaxed S/A layout pitch**  
- Even WL coupling
History (cont’d)

• **64K DRAM (’80, conference’79)**
  - Many changes at once - no dominant design
  - Standardized, Page mode, Refresh functions
  - $V_{cc}=5\text{v}$ only, $V_{ss}=0\text{v}$, Internal $V_{bb}$, $Trac=200\text{ns}$
  - Boosted wordline, Active restore

• **256K DRAM (’83, conference’82)**
  - 1Tr NMOS, 3P1M(FJ), I.I. mask increasing
  - $V_{cc}=5\text{v}$ only, Nibble/SC/CBR func., $Trac=150\text{ns}$
  - Open v.s. Folded, Redundancy, CMOS prototype
  - $Vdd$ bitline pre-charge
  - Some ASM, Wide I/O (x4)

• **1M DRAM (’86, conference’84)**
  - N-well CMOS, 3P1M, $V_{dd}/2$ cell plate
  - Half $V_{dd}$ bitline reference and pre-charge,
  - Shared folded bitline
  - x4/x8, Package and module variety, Test circuits

• **4M DRAM (’89, conference’87)**
  - 3D stacked or trench cell, CMOS, 4P1M,
  - x16, Fast page/Self refresh, $Trac=80\text{ns}$
  - Current-mirror data bus amp., Boosted I/O driver
  - Word line strapping, Triple-well
**Basic Bitline Structure (2)**

- **Folded Shared**
  - Less area occupied by S/As
  - Used in nearly all 16M
  - Relaxes S/A pitch

- **Interleaved (Multiplexed)**

**History (cont’d)**

- **16M DRAM (’92, conference’90)**
  - N-well CMOS, 4P2M
  - Internal Vdd down-converter (5v ext.---3.3v int.)
  - Shared Y-decoder, Interleaved S/A,
  - Vpp supply WL driver, RDRAM(PLL/DLL)

- **64M DRAM (’95, conference ’91)**
  - Triple well CMOS, Vss Substrate, 4P2M,
  - Vdd=3.3v, Separate I/O PS-pin (Vddq/Vssq)
  - SDRAM (clocked In, pipelined, burst I/O, term. I/F)
  - COB, Staggered Sense amp.
Circuit Evolution Picking up

- 3Tr to 1Tr1C
- Boosted Wordline
- Single Power Supply • NMOS to CMOS (Vbb gene., WL boost)
- Redundancy
- Vdd/2 BL pre-charge
- Internal DC converter
- Clocked operation
- PLL/DLL
- Multi-bank core
- Address Multiplex
- Open BL to Folded BL
- Page & Refresh Mode
- Appli. Specific Circuits (ex. SR for VRAM)
- Test mode
- Pipelined operation
- High speed interface
- Embedded core

Cell Array and Circuits

(1) 1 Transistor 1 Capacitor Cell
• Size Comparison to SRAM Cell

(2) Array Example

(3) Major Circuits (today’s example)
• Sense amplifier
• Dynamic Row Decoder
• Wordline Driver

The other circuits interesting for VLSI designer
• Data bus amplifier • Voltage Regulator
• Reference generator • Redundancy technique
• Replica technique • High speed I/O circuits
**SRAM v.s. DRAM**

6Tr embedded SRAM

- **Gain element in cell**

1Tr1C Standard DRAM

- **Passive element**
  - (No gain, Refresh needed)

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**Comparison of SRAM and DRAM Cell Size**

- **6Tr SRAM**
- **3Tr**
- **Stack DRAM**
- **Plainer**

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Standard DRAM Array Design Example

64 Mbit Core, a part of 256M DRAM

32 Mbit

32 Mbit

64 Mbit DRAM consists of two 32 Mbit arrays

8 global data buses

8 global data buses and 8 amplifiers

32 Mbit array.
DRAM Design Overview

DRAM Array Example (cont’d)

Interleaved S/A & Hierarchical Row Decoder/Driver
(shared bit lines are not shown)

512K Array \( \text{Nmat}=16 \) or 12
(256 WL x 2048 SA)

Row Decoder and Driver

<WL Strapping Type>

Addresses
Reset
Dynamic NAND

VCC
WDi

Contact only (Strapping)
AL strap line
P1 word line
Row Decoder and Driver (cont’d)

<Hierarchical WL Type>

Addresses
Reset
Dynamic NAND
Negative Voltage?

Sense Amplifier Circuits - Folded Shared Interleaved -
Standard DRAM Design Feature

- Tightly depends on technology
- The row circuits is fully different from SRAM.
- Few product variation in the same technology
- “Trends” is mother, “Cost” is father.
- “Standard” gives us less freedom!
- Almost always analogue circuit design
- Simply forward critical path
- CAD: Spice-like circuits simulator

  Fully handcraft layout,
  Whole-chip tools must be a dream.
Embedded DRAM or Merged D&L

- Merged DRAM and Logic
  - Technology choice and cost issue
    ---- People have talked too much above.
  - Otherwise, that’s a near future evolution.
- Current Technology behind advanced DRAMs’
- Small ASIC seems to be not yet on the business.
- How solve the following technical problem?
  memory wall, granularity, I/O power

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Speed Gap between DRAM and CPU
- Memory Wall -

Performance (Speed Ratio)

Year

80 85 90 95 00

DRAM 7%/year

μ PU
60%/year

Increasing The Gap
The numbers of DRAM on PCs

<table>
<thead>
<tr>
<th>Main Memory Size</th>
<th>4MB</th>
<th>8MB</th>
<th>16MB</th>
<th>32MB</th>
<th>64MB</th>
<th>128MB</th>
<th>256MB</th>
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<tbody>
<tr>
<td>DRAM Generation</td>
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<td>89</td>
<td>93</td>
<td>97</td>
<td>01</td>
<td>05</td>
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<tr>
<td>1Mb</td>
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<td>16</td>
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<td>16</td>
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<td>8</td>
<td>2</td>
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Memory/DRAM growth @60%/year
Memory/System growth @25%/year

Macro Power (MDL v.s. Standard DRAM)

- External Standard DRAM
- 0.35um 8M Macro
- 2.35W I/O Load Charging
- 1.11W Re-design
- 70% Re-design
Macro Power (cont’d)

75% Macro Power depends on the numbers of I/O

External use of Standard DRAM

Load 50 pF

Power [W]

Load 1 pF

75%

15%

1.11W

0.78W

2.35W

Macro Re-design & Shrink on I/O No.

depend on I/O No.

depend on I/O No.

individual

The First Commercial Product of Embedded DRAM

M32R/D (Mitsubishi)

- 0.45μm DRAM
- 32-bit RISC CPU
  + 16Mbit DRAM
- Die Size: 153.7mm²
0.25um Embedded DRAM Products

DRAM Design Overview

Memory Density and Logic Gates

- Affordable DRAM-density & Logic-gates in a 100mm² Die

Standard DRAM Technology

MDL Technology

Pure Logic Technology

MDL Process

SRAM

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**DRAM Design Overview**

**DRAM Macro Size Shrink**

Which could make cost effective?

<table>
<thead>
<tr>
<th>DRAM Macro Area (mm²)</th>
<th>Rule (μm)</th>
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<tbody>
<tr>
<td>16Mb</td>
<td>0.50</td>
</tr>
<tr>
<td>8Mb</td>
<td>0.35</td>
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<tr>
<td>32Mb</td>
<td>0.25</td>
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<tr>
<td>100</td>
<td>0.18</td>
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</table>

Cost Effective Region?

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**Application Specific Memory**

-Brief Introduction-

- Various ASM introduced since ’83
  - VRAM: 64K to 4M VRAM
  - Field Memory (NEC), Triple Port (FJ)
  - mostly for ASICs or conference chips
- Only VRAM got a semi-standardization
- Longer design TAT
  as more complicated spec. and circuits
- Redundancy and Test issues: big problems
- Never major products

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**256K Dual Port Video RAM**

**(a) Conventional 2D Graphic System**

- Standard DRAM
- Parallel to Serial
- CPU
- Time Share
  - CPU efficiency 50%

**(b) 2D Graphic System used VRAM**

- Conditional Dual Port
  - 1024 bit transfer @100ns
  - CPU efficiency 95%

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**256K Dual Port Video RAM (cont’d)**

- Narrow pitch matched SAM (or Sift Register) design
- No explicit bus for a mass of data transfer at a time
- A hinted solution by utilizing a memory parallelism
4M bit Cubic Memory (conference ’90)

- 16b x 16b x 16b (4Kbit) virtual bit map space
- six different ways of column access on the fly access

Summary

- Passive 1Tr1C cell leads all the features of dynamic circuits and design complexity.
- The row circuits is fully different from SRAM.
- A Dinosaur, Standard DRAM, become almost dead, because of both the technology saturation and the narrow band-width itself.
- The design technique should be transferred for the coming embedded era.