John Douglas Owens

Gates Hall 3B Room 396 Stanford, CA 94305-9035
650-725-3648 / jowens@graphics.stanford.edu

EDUCATION

Stanford University — Stanford, California
Department of Electrical Engineering — 1995–2002
Ph.D., Electrical Engineering, expected October 2002
M.S., Electrical Engineering, March 1997
Advisors: Professors William J. Dally and Patrick Hanrahan
Dissertation Topic: "Computer Graphics on a Stream Architecture"

University of California, Berkeley — Berkeley, California
Department of Electrical Engineering and Computer Sciences — 1991–1995
B.S., Highest Honors, Electrical Engineering and Computer Sciences, June 1995

RESEARCH INTERESTS

Computer systems: computer architecture, graphics and graphics architectures; media processors, applications, and algorithms; hardware-software design and APIs.

EXPERIENCE

Stanford University — Stanford, California
Research Assistant — 1997–2002
An architect of the Imagine Stream Processor under the direction of Professor William J. Dally. Responsible for major portions of hardware and software design for Imagine and its tools and applications.

Stanford University — Stanford, California
Teaching Assistant — Fall 2001
Teaching assistant for Computer Science 99S, "The Coming Revolution in Computer Architecture", under Professor William J. Dally. Designed course with Professor Dally, including lecture topics, readings, and laboratories.

Interval Research Corporation — Palo Alto, California
Consultant — 1997–2000
Investigated new graphics architectures under the direction of Dr. Matt Regan.

Stanford University — Stanford, California
Research Assistant — 1995–1997
Under the direction of Professor Patrick Hanrahan, designed and built the Lightning distributed framebuffer.

Silicon Studio, Silicon Graphics Inc. — Mountain View, California
Software Engineer — Summer 1995
Performed development work on SGI's Firewalker video-game authoring system, mastering game titles to game platforms.

University of California, Berkeley — Berkeley, California
Teaching Assistant — Spring 1995
Teaching assistant for Computer Science 150, "Digital Design", under Professor Richard Newton. Responsible for laboratory section, office hours, grading, and midterm review.

Intel Corporation, P7 Architecture Group — Santa Clara, California
Design Engineer — Summer 1994
Designed and implemented graphical user interface to Intel's Sphinx microarchitecture simulator.

First Person Inc. (subsidiary of Sun Microsystems Inc.) — Palo Alto, California
Hardware Designer — Summer 1993
Assisted in design of NTSC SBus-compatible framebuffer.

PUBLICATIONS

Brucek Khailany, William J. Dally, Scott Rixner, Ujval J. Kapasi, John D. Owens, and Brian Towles. "Exploring the VLSI Scalability of Stream Processors". To appear in the Proceedings of the 9th International Symposium on High-Performance Computer Architecture, Feb. 8–12, 2003.

Ujval J. Kapasi, William J. Dally, Brucek Khailany, John D. Owens, and Scott Rixner. "The Imagine Stream Processor". Proceedings of the IEEE International Conference on Computer Design, Sept. 16–18, 2002, pp. 282–288.

John D. Owens, Ujval J. Kapasi, Peter Mattson, Brian Towles, Ben Serebrin, Scott Rixner, and William J. Dally. "Media Processing Applications on the Imagine Stream Processor". Proceedings of the IEEE International Conference on Computer Design, Sept. 16–18, 2002, pp. 295–302.

Ben Serebrin, John D. Owens, Brucek Khailany, Peter Mattson, Ujval J. Kapasi, Chen H. Chen, Jinyung Namkoong, Stephen P. Crago, Scott Rixner, and William J. Dally. "A Stream Processor Development Platform". Proceedings of the IEEE International Conference on Computer Design, Sept. 16–18, 2002, pp. 303–308.

John D. Owens, Brucek Khailany, Brian Towles, and William J. Dally. "Comparing Reyes and OpenGL on a Stream Architecture". 2002 SIGGRAPH / Eurographics Workshop on Graphics Hardware, Sept. 1–2, 2002, pp. 47–56.

Ujval J. Kapasi, Peter Mattson, William J. Dally, John D. Owens, and Brian Towles. "Stream Scheduling." Proceedings of the 3rd Workshop on Media and Streaming Processors, Dec. 2, 2001, pp. 101–106.

Brucek Khailany, William J. Dally, Scott Rixner, Ujval J. Kapasi, Peter Mattson, Jin Namkoong, John D. Owens, Brian Towles, and Andrew Chang. "Imagine: Media Processing with Streams." IEEE Micro, March/April 2001, pp. 35–46.

Ujval J. Kapasi, William J. Dally, Scott Rixner, Peter R. Mattson, John D. Owens, and Brucek Khailany. "Efficient Conditional Operations for Data-parallel Architectures". Proceedings of the 33rd Annual Symposium on Microarchitecture, Dec. 10–13, 2000, pp. 159–170.

Peter Mattson, William J. Dally, Scott Rixner, Ujval J. Kapasi, and John D. Owens. "Communication Scheduling". Proceedings of the Ninth International Conference on Architectural Support for Programming Languages and Operating Systems, Nov. 12–15, 2000, pp. 82–92.

Brucek Khailany, William J. Dally, Scott Rixner, Ujval J. Kapasi, Peter Mattson, Jin Namkoong, John D. Owens, and Brian Towles. "Imagine: Signal and Image Processing Using Streams". Hotchips 12, August 2000.

John D. Owens, William J. Dally, Ujval J. Kapasi, Scott Rixner, Peter Mattson, and Ben Mowery. "Polygon Rendering on a Stream Architecture". 2000 SIGGRAPH / Eurographics Workshop on Graphics Hardware, August 2000. pp. 23–32.

Scott Rixner, William J. Dally, Ujval J. Kapasi, Peter Mattson, and John D. Owens. "Memory Access Scheduling", 27th Annual International Symposium on Computer Architecture, June 2000. pp. 128–138.

Scott Rixner, William J. Dally, Brucek Khailany, Peter Mattson, Ujval J. Kapasi, and John D. Owens. "Register Organization for Media Processing", Proceedings of the 6th International Symposium on High-Performance Computer Architecture, Jan. 10–12, 2000, pp. 375–386.

Scott Rixner, William J. Dally, Ujval J. Kapasi, Brucek Khailany, Abelardo Lopez-Lagunas, Peter R. Mattson, and John D. Owens. "A Bandwidth-Efficient Architecture for Media Processing", Proceedings of the 31st Annual International Symposium on Microarchitecture, Nov. 30–Dec. 2, 1998, pp. 3–13.

PATENTS

US 6269435: System and method for implementing conditional vector operations in which an input vector

containing multiple operands to be used in conditional operations is divided into two or more output vectors based on a condition vector. William J. Dally, Scott Whitney Rixner, John Owens, Ujval J. Kapasi. Issued 31 July 2001.

INVITED TALKS

Sony Research Laboratory, NVIDIA Corporation, Intel Media Research Laboratory, Interval Research Corporation, UCLA, UC Davis, UCSD, Sacramento State University, San Francisco State University.

ACTIVITIES AND HONORS

Stanford Computer Systems Laboratory Bureaucrat (student representative to faculty), 1996–2000
Stanford Program for Academic Excellence Mentor, 1997–2000
Stanford Women's Intercollegiate Water Polo Volunteer Assistant Coach, 1999–present
Stanford College of Engineering Lawrence R. Thielen Memorial Fellowship
Charles Mills Gayley Fellowship for Graduate Study
Eta Kappa Nu (Mu Chapter)
Tau Beta Pi (California Alpha Chapter)
University of California, Berkeley Men's Intercollegiate Water Polo, 1991–1994
Order of the Golden Bear, University of California, Berkeley
University of California, Berkeley Regents and Alumni Scholar
National Merit Scholar
United States Presidential Scholar
Eagle Scout, Boy Scouts of America